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3	PhD Thesis Title	TIQ Technique Based Low Power Flash Analog to Digital Converter	
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7	Brief synopsis This thesis addresses the design of Flash ADC using Threshold Inverter Quantizer (TIQ) Comparator, Quantized Differential (QD) Comparator, CMOS Linear Tunable Transconductance Element (CMOS-LTE) Comparator and Leakage Current Threshold (LCT) Comparator. The TIQ comparator uses two cascaded inverters as a voltage comparator and the QD Comparator uses Differential amplifier with cascaded inverters as a comparator. The TIQ Comparator is single ended and is very sensitive to power supply noise. The power dissipation in QD Comparator is relatively more. To overcome these problems, CMOS-LTE Comparator has been designed, which improves the Power Supply Rejection Ratio (PSRR) and also reduces the power dissipation. Reference voltages in all these comparators are generated by systematically sizing the transistors of the comparators, thus completely eliminating the resistive ladder network required for the architecture. The thesis also discusses LCT Comparator that uses the TIQ concept and leakage current for the generation of reference voltages. Accordingly, it is observed that, there is a substantial improvement in the PSRR and power dissipation. Finally the Optimized Flash ADC design with $2^n/2$ comparators is discussed.		